cont. B2

85. (New) The method in claim 81, wherein exposing the conductive layer to a thermal process comprises exposing the conductive layer to an alloy process.--

REMARKS

Claims 36-39 and newly added claims 76-85 are currently pending in the present application. In the Office Action mailed April 12, 2001, the Examiner rejected claims 36-37 under 35 U.S.C. § 102 (e) as being anticipated by United States Patent No. 6,165,802 to Cuchiaro *et al.* ("Cuchiaro"), and also rejected claim 36 along with claims 38-39 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 5,726,083 to Takaishi ("Takaishi").

Applicant's invention exposes a conductive layer to an oxygen-inhibiting plasma prior to the formation of the another layer or layers on the conductive layer to substantially reduce the association of oxygen with the conductive layer during formation of the other layer or layers. By reducing the amount of oxygen associated with the conductive layer, the electrical characteristics of a semiconductor device including the conductive layer are improved, as will be discussed in more detail below with reference to the disclosed embodiments of the invention. The disclosed embodiments of the invention are discussed in comparison to the applied references in order to help the Examiner appreciate certain distinctions between the pending claims and the subject matter of the applied reference. Specific distinctions between the pending claims and the applied reference will be discussed after the discussion of the disclosed embodiments and the applied reference. This discussion of the differences between the disclosed embodiments and applied reference does not define the scope or interpretation of any of the claims.

Figures 4 and 5 illustrate in-process semiconductor devices being formed by a process according to one embodiment of the present invention. As mentioned in the specification, for the purposes of explanation the in-process semiconductor device is assumed to be a capacitor in the process of being constructed. In Figure 4, the capacitor includes a first conductive layer or 24, which may be formed from hemispherical silicon grain (HSG), formed over a substrate 22, and a dielectric 26 formed on the first conductive layer. In the examples of Figures 4 and 5, the dielectric 26 is formed from tantalum pentoxide Ta_2O_5. A second

conductive layer 28 formed from tungsten nitride WN_x is then formed on the dielectric 26. The tungsten nitride layer 28 has a tendency to associate with oxygen, particularly if that layer is exposed to oxygen prior to a third conductive polysilicon layer 30 being formed on the tungsten nitride layer 28. During subsequent processing of the capacitor, the oxygen contained in the tungsten nitride layer 28 can combine with silicon from the polysilicon layer 30 to form an unwanted silicon dioxide layer 36 between the tungsten nitride layer 28 and the polysilicon layer 30. For example, a thermal process step such as the formation of a borophosphosilicate glass (BPSG) layer 34 over the polysilicon layer 30, which of course occurs after the formation of the polysilicon layer 30, may cause a reaction between the polysilicon layer 30 and the oxygen in the tungsten nitride layer 28 and thereby form the silicon dioxide layer 36.

Ideally, the HSG layer 24 forms a first plate of the capacitor, the tantalum pentoxide 26 forms the dielectric of the capacitor, and the tungsten nitride layer 28 and polysilicon layer 30 form the second plate of the capacitor. With the formation of silicon dioxide layer 36, however, the capacitor now includes a first capacitor corresponding to the HSG layer 24, tantalum pentoxide 26, and tungsten nitride layer 28, and a second capacitor in series with the first capacitor, with the second capacitor corresponding to the tungsten nitride layer 28, silicon dioxide layer 36, and polysilicon layer 30. These first and second capacitors connected in series have a combined capacitance that is less than that of the ideally formed capacitor. As will be understood by those skilled in the art, the thickness of the silicon dioxide layer 36 affects the value of the combined capacitance.

In the capacitor of Figure 4, the thickness of the silicon dioxide layer 36 is greatly reduced by exposing the tungsten nitride layer 28 to an oxygen-inhibiting agent prior to the formation of the polysilicon layer 30 to thereby greatly reduce the association of the tungsten nitride layer with oxygen. The silicon dioxide layer 36 in the embodiment of Figure 4 is less than 10 angstroms thick due to the oxygen-inhibiting agent, while in a conventional capacitor shown in Figure 3 the silicon dioxide layer 36 is about 10-40 angstroms thick. In the capacitor of Figure 5, the exposure of the tungsten nitride layer 28 to the oxygen-inhibiting agent eliminates the formation of the silicon dioxide layer 36 altogether.

The oxygen-inhibiting agent may be an N_2 and H_2 plasma, with the tungsten nitride layer 28 ideally being exposed to this plasma prior to exposing tungsten nitride layer to an

atmosphere associated with the formation of the polysilicon layer 30 or prior to exposing the tungsten nitride layer to oxygen. As described in the specification, it is believed the exposure of the tungsten nitride layer 28 to the N_2 and H_2 plasma or any of the other oxygen-inhibiting agents stuffs the tungsten nitride layer grain boundaries with nitrogen or otherwise passivates the tungsten nitride layer, making the bonds at the grain boundaries less active and less likely to associate with oxygen. It should be noted that even if the tungsten nitride layer 28 is exposed oxygen, the layer may thereafter be exposed to a reducing atmosphere, such as silane gas SiH4, prior to formation of the polysilicon layer 30 to thereby reduce the oxygen content of the tungsten nitride layer 28 and reduce the thickness of any silicon dioxide layer 36 thereafter formed.

In another embodiment discussed with reference to Figure 6, a first conductive layer such as a tungsten nitride layer 128 is deposited over a substrate 122 and a dielectric layer 126, such as a tantalum pentoxide layer, is deposited over the tungsten nitride layer. In this situation, the deposition of the tantalum pentoxide layer 126 may cause the tungsten nitride layer 128 to incorporate oxygen, reducing the capacitance of a capacitor including the tungsten nitride layer and tantalum pentoxide layer. Accordingly, in this embodiment of the invention, the tungsten nitride layer 128 is exposed to a N_2 and H_2 plasma or other oxygen-inhibiting agent before depositing the tantalum pentoxide layer 126. As previously described, the N_2 and H_2 plasma passivates the tungsten nitride layer 128 to thereby prevent oxygen from being incorporated within the tungsten nitride layer.

Another embodiment of the present invention is discussed with reference to Figures 7-10 in which and interposing layer 52 such as a tungsten nitride layer 52 is formed between a conductive line material 48 to enhance the electrical contact between the line material and the plug, promote adhesion of the line material within a container 50, prevent or slow the diffusion of materials across the tungsten nitride layer boundary, or serve some other purpose. As previously described, the tungsten nitride layer 52 may associate with oxygen after it is formed and subsequent thermal processes may result in the formation of an oxide layer 54 formed between the tungsten nitride layer 52 and the line material 48. Because the oxide layer 54 is an insulator, this layer will adversely affect the electrical connection between the line material 48 and the plug 46. By exposing the tungsten nitride layer 52 to an oxygen-inhibiting

agent or a reducing atmosphere prior to formation of the line material 48, the thickness of the oxide layer 54 is reduced to a thickness of less than 10 angstroms or entirely eliminated as illustrated respectively in Figures 9 and 10. Thus, in all embodiments a conductive layer is exposed to an oxygen-inhibiting agent or reducing atmosphere prior to another layer being formed on the conductive layer to thereby reduce an ability of the conductive material to associate with oxygen.

The Cuchiaro patent discloses a method of fabricating an integrated circuit that includes a ferroelectric element, such as a dielectric in a capacitor. Ferroelectric elements are utilized in forming capacitors that function as nonvolatile storage elements in nonvolatile integrated circuit memories. Referring to Figure 1, such a capacitor 118 includes a bottom electrode 120, a ferroelectric thin film 122 formed over the bottom electrode as the dielectric of the capacitor, and a top electrode 124 formed over the ferroelectric thin film. The electrical characteristics of ferroelectric thin film 122, such as high residual polarization, good coercive field, high fatigue resistance, and low leakage currents make them suitable for such applications. Cuchiaro is particularly directed towards restoring the favorable electrical characteristics of the ferroelectric thin film 122 that are degraded during the step of hydrogen annealing that occurs as part of the formation of an integrated circuit including the capacitor 118 on a wafer 140. During the formation of a MOSFET 113 in the wafer 140, a silicon substrate 102 in which the MOSFET is formed experiences numerous defects in the single crystal structure of the substrate, which lead to the deterioration of the desired electrical characteristics of the MOSFET. These defects arise, for example, from such steps as ion implantation and high energy steps such as ion-mill and plasma etching.

Hydrogen annealing utilizes the reducing property of hydrogen to eliminate the defects in the silicon substrate 102, such as dangling bonds, and thereby restore the desired electrical characteristics of the MOSFET 113. Unfortunately, the use of hydrogen annealing in restoring the desired electrical characteristics of the substrate 102 and MOSFET 113 has the unfortunate consequence of deteriorating the desired electrical properties of the ferroelectric thin film 122. This occurs due to the diffusion of hydrogen through the top electrode 124 and through the sides of the capacitor 118 to the ferroelectric thin film 122, which reduces the oxide

contained in the ferroelectric thin film and has other negative affects on the desired electrical properties of the thin film.

Figure 2 in Cuchiaro is a flow diagram that illustrates a process for reversing the detrimental affects of hydrogen annealing on the ferroelectric thin film 122. This process will now be described with reference to Figures 1 and 2. In the process of Figure 2, steps 212-226 are the steps in which the bottom electrode 120 and ferroelectric thin film 122 are formed. Note that in step 226, which occurs prior to step 228 in which the top electrode 124 is formed, the ferroelectric thin film 122 is annealed in oxygen to form the desired ferroelectric thin film 122. After the ferroelectric thin film 122 is annealed in oxygen in step 226, the top electrode 124 is formed on the thin film in step 228 and a hydrogen barrier layer 126 (Figure 1) may then be formed over the top electrode 124 in step 230. The hydrogen barrier layer 126 inhibits the diffusion of hydrogen into the ferroelectric thin film 122 during subsequent hydrogen annealing of the wafer 140 (Figure 1) in step 232. The hydrogen annealing in step 232 may be performed using an H_2 and N_2 mixture as described in column 10, lines 43-45.

As previously described, the hydrogen annealing step 232 eliminates defects in the silicon substrate 102 such as dangling bonds and thereby restores the desired electrical characteristics of the MOSFET 113 but also detrimentally affects the electrical characteristics of the ferroelectric thin film 122 due to the diffusion of hydrogen into the ferroelectric thin film. In step 234, the wafer 140 is subjected to an oxygen-recovery anneal to restore the electrical properties of ferroelectric thin film 122 that were degraded due to the hydrogen annealing in step 232. The oxygen-recovery anneal and possibly other steps reverse the degradation of the electrical properties of the ferroelectric thin film 122 by reoxidizing chemical compounds in the ferroelectric thin film. *See* column 9, lines 5-17. The oxygen-recovery anneal of step 234 may be utilized to restore the desired electrical properties of the ferroelectric thin film 122 even with hydrogen barrier layer 126 is not formed over the top electrode 124. In Cuchiaro, it is the oxygen-recovery anneal and any other processing in step 234 that restores the desired electrical properties of the ferroelectric thin film 122 and thereby allows the capacitor 118 to be utilized in nonvolatile memory applications.

In Cuchiaro, the hydrogen annealing step does not "expose" either the bottom electrode 120 nor the top electrode 124 to an oxygen-inhibiting agent as that term in used in

present application. Cuchiaro does not disclose passivating either of the conductive electrodes 120, 124 by directly exposing the electrode to an oxygen-inhibiting agent or reducing atmosphere prior to another layer being formed on the electrode. Instead, in Cuchiaro after the bottom and top electrodes 120, 124 are completely formed, the resulting structure is hydrogen annealed to achieve the purpose of hydrogen annealing (*i.e.*, to correct defects in the underlying substrate 102 created during formation of the nonvolatile memory cell). Note that if the top electrode 124 includes multiple layers, all of these layers are formed prior to the hydrogen annealing, with no individual layer being passivated prior to the formation of the another layer thereon.

It should be noted that in Cuchiaro, prior to the hydrogen annealing in step 232, the bottom electrode 120, ferroelectric thin film 122, and top electrode 124 may be exposed to oxygen individually or in groups as the respective layers are formed, with one example being the annealing of the ferroelectric thin film 122 in oxygen as discussed above. Thus, if the bottom electrode 120 was, for example, tungsten nitride then this tungsten nitride layer could associate with oxygen during the oxygen annealing in step 232. Furthermore, it should be noted that none of the embodiments of Cuchiaro disclose or suggest passivating a conductive layer prior to the formation of another layer on that layer, including the test example described with reference to Figure 4 in which a thin film capacitor 400 is annealed in an H_2 and N_2 mixture, as discussed in column 10, lines 15-67. The capacitor 400 is annealed in the H_2 and N_2 mixture after a bottom electrode 420, ferroelectric thin film 422, and a top electrode layer 424 have been formed, as would actually occur when the capacitor is being formed in an actual device like the nonvoltatile memory cell of Figure 1. Thus, if the top electrode layer 424 include were to include a tungsten nitride and polysilicon layer, then both these layers would be formed prior to the annealing of capacitor 400.

The Takaishi patent discloses a process for reducing the leakage current through a capacitor having a tantalum oxide dielectric by limiting the temperature of heat treatments performed subsequent to the formation of the tantalum oxide dielectric during the formation of a memory cell including the capacitor. In the "Description of the Related Art" section of Takaishi, a conventional process for forming a dynamic random access memory is discussed. This description discusses various conventional process steps, including the ion implantation of

phosphorous into n-type drain regions of n-channel enhancement type field effect transistors (FETs) in a silicon substrate, and the ion implantation of boron fluoride into p-tupe drain regions of p-channel enhancement type FETs in the substrate. *See* column 3, lines 39-46. A titanium layer and a titanium nitride layer were then deposited over an entire surface of the memory cell being constructed (*i.e.*, in-process memory cell), including over the n-type and p-type drain regions, and the in-process memory cell is placed in a nitrogen ambience and subjected to rapid annealing at 690 degrees centigrade for 30 seconds. *See* column 3, lines 48-53. This converts the titanium on the p-type and n-type drain regions into titanium silicide films, which serve as barrier metal layers over the p-type and n-type shallow junction drain regions. *See* column 3, lines 53-56. Tungsten contacts are thereafter formed on the barrier metal layers. *See* column 4, lines 15-24.

In Takaishi, the titanium and titanium nitride layers are placed in a nitrogen atmosphere for rapid annealing and are not placed in an oxygen-free atmosphere to passivate the surface of these layers and reduce the ability of the layers to associate with oxygen. Such annealing is performed to convert the titanium and titanium nitride layers into titanium silicide films which function as barrier metal layers over the drain regions. Such barrier metal layers prevent damage to the drain regions during the subsequent formation of the tungsten contacts, as is understood by those skilled in the art. There is no disclosure no suggestion in Takaishi of a process to provide an atmosphere for passivating the titanium and titanium nitride layers. Instead, Takaishi merely discloses an atmosphere suitable for performing the desired rapid annealing to form the titanium silicide barrier metal layers.

Amended claim 36 recites a method of forming a semiconductor device including depositing a first conductive layer having a surface and having an ability to associate with oxygen, incorporating an oxygen-free material directly into the surface to passivate the surface of the first conductive layer to reduce the ability of the first conductive layer to associate with oxygen, depositing a second conductive layer on the surface after incorporating the oxygen-free material into the surface, and exposing the second conductive layer to a thermal process. Neither Cuchiaro nor Takaishi discloses or suggests the recited operations, including passivating the first conductive layer. The combination of elements recited in claim 36 is therefore allowable.

New claim 76 recites a method of forming a semiconductor device including depositing a tungsten nitride layer having a surface, incorporating an oxygen-free material directly into the surface of the tungsten nitride layer to passivate the surface of the tungsten nitride layer to reduce an ability of the tungsten nitride layer to associate with oxygen, depositing a conductive layer on the surface of the tungsten nitride layer after incorporating the oxygen-free material into the surface of the tungsten nitride layer, and exposing the conductive layer to a thermal process. Neither Cuchiaro nor Takaishi discloses or suggests incorporating an oxygen-free material directly into the surface of the tungsten nitride layer to passivate the surface of the tungsten nitride layer to reduce an ability of the tungsten nitride layer to associate with oxygen in combation with the other process operations recited in claim 76. The combination of elements recited in claim 76 is therefore allowable.

New claim 81 recites a method of forming a semiconductor device, including providing a first conductive layer having a surface and having an ability to associate with oxygen, placing the surface of the first conductive layer in direct contact with an oxygen-free atmosphere under appropriate conditions to passivate the surface and reduce the ability of the first conductive layer to associate with oxygen, providing a second conductive layer on the surface of the first conductive layer, and subjecting the second conductive layer to a thermal process. Once again, neither Cuchiaro nor Takaishi discloses or suggests the recited operations, and the combination of elements in claim 81 is therefore allowable.

Independent claims 36, 76, and 81 are allowable for the reasons set forth above with regard to each claim. The claims dependent on the independent claims are also allowable because of their dependency on the patentable independent claims, and because of the additional limitations added by the dependent claims.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned "**Version with Markings to Show Changes Made**".

The present patent application is in condition for allowance. Favorable consideration and a Notice of Allowance are respectfully requested. The Examiner is requested to contact the undersigned at the number listed below for a telephone interview if, upon

consideration of this amendment, the Examiner determines any pending claims are not in condition for allowance.

Respectfully submitted,

DORSEY & WHITNEY LLP

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PFR:asw

Enclosures:
Postcard
Check
Fee Transmittal Sheet (+ copy)
Revocation and Substitute Power of Attorney
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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the claims:

Claim 36 has been amended as follows:

36. (Amended) A method of forming a semiconductor device, comprising:

depositing a first conductive layer having a surface and having an ability to associate with oxygen;

incorporating an oxygen-free material directly into said surface to passivate the surface of said first conductive layer to reduce the ability of the first conductive layer to associate with oxygen;

depositing a second conductive layer on said surface after incorporating the oxygen-free material into the surface; and

exposing said second conductive layer to a thermal process.